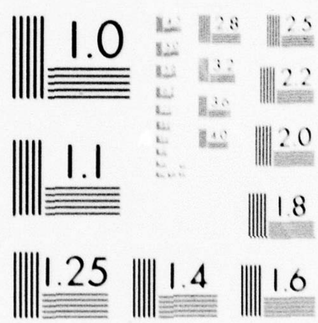
AD-A057 251 NORTHEASTERN UNIV BOSTON MASS ELECTRONICS RESEARCH LAB F/G 9/5
A DIGITAL CONTROL UNIT FOR A ROCKET BORNE QUADRUPOLE MASS SPECT--ETC(U)
APR 78 J S ROCHEFORT, R SUKYS F19628-76-C-0256
UNCLASSIFIED SCIENTIFIC-1 AFGL-TR-78-0106 NL

1 OF 1
AD
A057 251

END
DATE
FILMED
9-78
DDC



MICROCOPY RESOLUTION TEST CHART

NATIONAL BUREAU OF STANDARDS-1963-A

LEVEL II

(18)

AD A057251

AFGL-TR-78-0106

A DIGITAL CONTROL UNIT FOR A ROCKET BORNE QUADRUPOLE MASS SPECTROMETER

J. Spencer Rochefort
Raimundas Sukys

Northeastern University
Boston, Massachusetts 02115

Approved for public release; distribution unlimited.

April 1978

Scientific Report No. 1

AIR FORCE GEOPHYSICS LABORATORY
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
HANSCOM AFB, MASSACHUSETTS 01731

78 08 03 31

MIL-STD-847A
31 January 1973

Unclassified
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

18 19 REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: AFGL-TR-78-0106
2. GOVT ACCESSION NO.:
3. RECIPIENT'S CATALOG NUMBER:

4. TITLE (and Subtitle): 6 A DIGITAL CONTROL UNIT FOR A ROCKET BORNE QUADRUPOLE MASS SPECTROMETER.
5. TYPE OF REPORT & PERIOD COVERED: Scientific. Interim
6. PERFORMING ORG. REPORT NUMBER: Scientific Report No. 1

7. AUTHOR(s): 10 J. Spencer/Rochefort
Raimundas/Sukys
8. CONTRACT OR GRANT NUMBER(s): 15 F19628-76-C-0256

9. PERFORMING ORGANIZATION NAME AND ADDRESS:
Northeastern University
Electronics Research Laboratory
Boston, Massachusetts 02115
10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS:
61102F
16 2310G304 17 G3

11. CONTROLLING OFFICE NAME AND ADDRESS:
Air Force Geophysics Laboratory
Hanscom AFB, Massachusetts 01731
Monitor: Alan D. Bailey/LKD
12. REPORT DATE: 11 Apr[redacted]78
13. NUMBER OF PAGES: 33

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): 12 37p.
15. SECURITY CLASS. (of this report): Unclassified
15a. DECLASSIFICATION DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

14 Scientific-1

18. SUPPLEMENTARY NOTES

9 Scientific interim rept.,

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Digital Control
Programmable
Mass Spectrometer
Quadrupole

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

To control a quadrupole mass spectrometer during a rocket flight a programmable digital control unit has been developed. The design centers around a programmable read only memory. Up to eight different programs of 16 breakpoints may be sequentially selected. For data transmission, a PCM system has been included into the control unit. The operation and the circuits of the unit are described.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

78 08 03 31

127 500

alt

TABLE OF CONTENTS

TABLE OF ILLUSTRATIONS

I. INTRODUCTION

A rocket-borne quadrupole mass spectrometer is being developed by the Aeronomy Division of the Air Force Geophysics Laboratory. The design of the mass filter structures including the electron multiplier is pursued at the Laboratory. Northeastern University has been assigned the task to provide the mass filter with the necessary excitation and bias voltages and signal conditioning circuits.

The low altitude Cluster Ion Mass Spectrometer will measure masses from 1 to 255 amu's. The quadrupole will be excited with a 2.3 MHz RF signal of a peak amplitude in excess of 700 volts. It will be possible to switch the instrument into a positive or a negative ion mode of operation.

As a part of the electronics package, a programmable digital control unit has been developed. This unit exercises control over the generation of the excitation and bias signals. Also included are data conversion circuits. These circuits, in synchronism with the data gathering process, generate a PCM signal.

The operation of the control unit is based on a programmable read-only memory. Programs stored in the memory are selected in a pre-arranged sequence during the flight of the instrument. Since there are no command links contemplated for these flights, the sequence must be determined in advance. Only the number of times that each program will be repeated may be determined and set just

before the sounding rocket is elevated for the flight.

This report describes the control unit. In the first part of the report, a general description of the operations of the unit and of the functions that it controls is offered. Theoretical description of a quadrupole mass filter is beyond the scope of this report. Therefore, where necessary, only qualitative references are made to the various parameters that must be controlled for proper operation of the filter during a flight through the atmosphere. Also included is a description of the PCM system and its relationship to the data gathering process. The second part of the report presents a detailed description of the control unit, its circuits and the generation of the digital control signals.

II. OVERVIEW

The control unit of the rocket borne Cluster Ion Mass Spectrometer provides digital means to control the generation of the various analog signals required to operate the mass filter. In addition, the unit includes data conversion and signal conditioning circuits for the output signal of the filter. The spectrum information is conditioned for transmission over a telemetry link as an analog as well as a PCM signal.

A. FUNCTIONS TO BE CONTROLLED

The selection of a particular atomic spectral component by the quadrupole mass filter is accomplished through the control of the excitation signal. This signal, which is impressed upon the rods of the filter, consists of a dc and an RF component. The selected atomic mass unit (amu) is directly proportional to the amplitude, and inversely proportional to the square of the frequency of the RF voltage. The ratio between the dc and the ac components determines the selectivity of the instrument.

Usually the amplitude of the RF signal is varied to select the desired amu's while the frequency is kept constant. Aberrations of the mechanical as well as the electrical components preclude the use of a single, unique voltage level to select each individual spectral line. A small voltage range stepped or swept and hopefully centered around an amu is assigned to

each spectral line. Meanwhile, the ratio between the dc and the ac components of the excitation signal is experimentally adjusted to obtain reasonably good results. A ratio adjustment deemed to provide optimum results at one end of the spectrum may be completely unacceptable at the other end. Thus, a compromized adjustment results, unless the ratio can be controlled along the entire spectrum.

A number of bias voltages are required and must be controlled during the flight of the instrument. To overcome the vehicle potential, a bias signal is applied to the front end of the mass spectrometer. The ions entering the instrument are guided into the quadrupole structure by biased apertures and grids. Retarding or accelerating potentials are used to provide sufficient dwell time for the ions spiralling along the passageway between the rods. These bias voltages may be varied within the same polarity to achieve some desired results. Also, they must be reversed if the instrument is to switch between the positive and the negative modes of operation.

Sometimes it is desirable to obtain data about the presence of all ions above a certain amu. In that case, the instrument is switched into the so called total ions mode. In this mode, the dc component of the excitation signal is reduced to zero. Only the RF component remains and it may be kept constant or may be varied depending on the desired result.

B. METHODS OF CONTROL

The above described control over the operation of the mass filter during a flight is excercised by a number of preprogrammed digital signals. These digital commands either directly operate some analog switches or generate other digital signals. These in turn are converted into analog voltages by digital-to-analog converters and then are processed to the desired levels. A general block diagram of the control arrangement is shown in Figure 1.

The amu selection signal is generated by an up-counter. The counter is preset by an instruction with a count representing the beginning of an amu range through which the filter is to sweep. Then the counter is allowed to count until the end of that range is reached. The end of the count is signalled by another instruction which has been latched into a comparator circuit. A twelve-bit counter is used for this operation. Therefore, each instruction also consists of twelve bits; or a total of three bytes of memory must be used to generate a sweep. The status of the up-counter is continuously converted into an analog voltage, thus generating a staircase signal which controls the level of excitation at the quadrupole.

When several widely separated amu's have to be observed, a relatively long time is required to complete the sweep which continues through the regions of no interest. To save time, a mode

of operation is available in which the programmer sweeps through only a single amu range and then jumps to the start of another range. In this mode, a twelve-bit instruction is required to designate the start of each single amu sweep. An additional bit of an already available instruction byte used for other purposes is employed to switch the control unit into this mode of operation. Upon completion of the sweep for a given amu, the instruction indicating the start of the next amu sweep is selected. Thus 12 bits of memory, otherwise used to indicate the end of the sweep, are not needed. As it will become apparent later, a total of 32 bits of memory is saved by using this mode for a sweep through a single amu range.

The ratio control is exercised through an eight-bit instruction. The byte is applied in parallel to control a multiplying digital-to-analog converter.

The flight instructions for the mass spectrometer are stored in a one kilobyte EPROM. A binary counter is used to address the memory. When an end of a sweep or a step is reached, the counter is advanced through a count of four. The sequentially appearing contents of the addressed memory locations are stored into four eight-bit latches. The 32 outputs of the latches represent the control word. The first 12 bits of this word are used to instruct the up-counter. The next eight are used for ratio control. Other functions are controlled by the remaining 12 bits of the 32 bit control word.

In the mode of operation where the control unit steps through individual amu ranges, this one word is sufficient to exercise all of the control functions. However, in the sweep mode, the counter is immediately advanced through another count of four. During the first sequence of four, the up-counter, which generates the sweep control signal, is preset while the second sequence of four establishes the end of sweep information and updates the rest of the control signals. Since only 12 bits are required to preset the up-counter, the other 20 bits are essentially wasted in the first group of the four address locations. Although these locations could have been saved by an introduction of additional hardware, the programming of the memory would become somewhat more complicated. As it is, the last two least significant digits of the address are used to designate which byte of instructions is being stored in the memory. Also, the repetitive nature of the sequence provides an easy means to restore the control unit to a proper order, if, by chance, the address counter were to advance to the wrong count. The latching signals to store the output of the memory are derived from the same two bits of the address counter. Therefore, only the proper contents of the memory can be stored into the appropriate output latches. This, of course, cannot prevent the counter from being triggered by noise into different parts of the program, but the disastrous results of a single burst of noise completely destroying the mass spectrometer control program are prevented. Also included

is another safeguard. In the event that the address counter were to jump into an unprogrammed part of the memory, a signal is generated which resets the counter to the initial address of the program sequence.

Fewer than the 1024 bytes of available memory are needed to guide the mass filter through one complete data gathering cycle. Usually, the same program is repeated several times during a flight. Past experience has shown that 16 up-dates or break-points in the program were adequate for a rocket flight. Therefore, the unit is designed to store up to eight different programs of 16 break points. Only sequential program selection capability is provided. Once the required number of cycles for each program is determined, jumpers between appropriate pins of a connector are wired. The connector is installed into a receptacle provided for that purpose in the vehicle, and the control unit is programmed and ready for flight. Each cycle contains a number of 32-bit control words. One bit is used for the purpose of counting and its state will be the same in all but one word. The occurance of this exception is used to count the number of completed cycles. A total count of 256 for all eight programs must be accumulated before the first program is repeated again.

C. THE PCM

Although not directly associated with the control of the mass spectrometer, data conversion circuits are included within the control unit. The data from the mass filter section of the

instrument arrives in the form of a pulse train whose repetition frequency varies between 20 and 70 kpps. A frequency-to-voltage converter produces an analog signal varying between zero and minus ten volts. Inverted and halved, the analog signal goes to the subcarrier oscillator of the telemetry system. The original negative analog voltage is converted into a digital signal and transmitted over a PCM/FM/FM link.

The PCM NRZ-L data stream flows at 10 kHz rate. One complete frame is assigned to transmit data associated with each amu. The frame consisting of 120 bits starts with a 16-bit frame synchronization pattern which is followed by a 5-bit status monitor word and a 9-bit amu identification word. The remaining bits are divided into nine 10-bit spectrum data words. Complete synchronization is maintained at all times between the PCM and the control functions of the mass filter. One millisecond before the MSB of the frame synchronization pattern appears, a sync pulse signals the start of a voltage sweep through a new amu range. At this time, if any changes in the control functions of the instrument are required, the up-counter of the control unit is preset with new information. Any transients in the analog control voltages caused by the updating process have 3.8 milliseconds to settle before the next meaningful sample of the analog signal is converted into the digital word. With the onset of the frame synchronization pattern, the nine MSB's of the up-counter and the five system status bits are transferred into a shift

register to follow the synchronization word.

While the up-counter controlling the sweep signal is clocked every 750 μs, the analog data is sampled and converted into the digital signal once every millisecond. Therefore, the sweep staircase signal advances through five out of the sixteen levels assigned to one amu interval in the 3.8 ms before the first sample to be transmitted is taken. The conversion time is approximately 100 μs. The MSB of the first data word appears in the PCM pulse train 200 μs after the start of the conversion, or four milliseconds from the beginning of a sweep through a new amu range. Eight more samples are taken and transmitted before the next amu domain is entered. At this time, the whole pattern repeats itself.

III. CIRCUITS

The control unit has been designed mainly with C-MOS 4000 series integrated circuits. Notable exceptions are the 2758 EPROM and the circuits associated with the data conversion and monitor functions. The choice of the EPROM dictated a 5 volt supply operation for all of the digital circuits, while the analog units operate on ±15 volts.

The circuits of the mass spectrometer control unit may be subdivided into three main groups according to the function they perform. The Digital Control group generates the digital signals which control the analog sections of the mass spectrometer as well as some housekeeping functions of the control unit itself. The Data Conversion and Monitor Circuits process and condition the spectral information produced by the mass filter. They generate the PCM signal. They also produce and buffer various monitor signals originating either within the control unit or arriving from the analog circuits. The Sequencer group is used for the control of the control unit itself. It generates the command and clock pulses which trigger and synchronize various events in the other two groups.

A. DIGITAL CONTROL CIRCUITS

Digital signals which control the generation and/or switching of analog signals in the mass spectrometer originate in the group of circuits shown in Figure 2. This group includes memory, counters,

comparator and latching circuits. Although functionally belonging to the Data Conversion and Monitor classification, two digital-to-analog converter-monitor circuits are included in the circuit diagram.

The operation of the control unit in general and of this circuit group in particular is based on the 2758 EPROM. The commands to the mass spectrometer are stored in this one kilo-byte unit. Eight separate flight programs of a maximum length of 128 bytes each may be selected through the three most significant address lines A_9, A_8 and A_7. Since the three-bit address is generated by a counter located in the Sequencer section of the unit, the program selection is sequential. The contents of the memory within each program block are selected by the address counter (U18). The counter is incremented (A CLK) whenever an up-date of the control signal is required. Every time updating is requested, the counter is advanced through a count of either four or eight. The contents of the memory appearing sequentially on the output bus are stored, also sequentially, in the four 8-bit latches (U20 - U23) by pulses on lines S_1 through A_4. The outputs of these latches comprise the 32-bit control signal. The first four output lines are assigned to the bias control (spare, B_1, B_2, B_3). Lines designated as TI and P/N switch the mass spectrometer into the total ions and/or positive or negative ion operations. The eight bits from the next latch (U21) are assigned to the ratio control. The remaining bits

with the exception of SWP, PR, PM and a couple of spares are dedicated to control the presettable binary up-counter (U24 - U26). The digital number on these lines presets the up-counter whenever updating takes place, provided the PE signal is at ONE. The outputs of the counter (D_0 - D_{11}) control the generation of the staircase signal which, in turn, is used to control the generation of the quadrupole excitation signals.

When a ZERO is present on the SWP line, the updating process is initiated in the sequencer section and stops after the address counter has been advanced by a count of four. ONE on that line allows the address counter to continue its advance through another count of four. During this last count, the PE line remains at ZERO. Therefore, the new contents stored into the latches do not affect the up-counter. The whole count-of-eight updating process takes approximately 90 μs. The period of the AMU clock is 750 μs. Therefore, the counter remains at the preset count and does not advance until long after all of the analog circuits have received the new control inputs. When the up-counter reaches a count which has been stored in the latches U22 and U23 during the second part of the updating sequence, the output (designated as COMP) of the digital comparator (U27 - U29) jumps to ONE. This indicates to the sequencer sections of the control unit that the given task has been completed and a set of new instructions are in order.

The digital-to-analog converter (AD7520LD) and the operational amplifiers (U40) provide counter status information in an analog

form. Only eight MSB's are monitored. Since the instrument is designed to cover the range of up to 255 amu's, these eight bits provide the information needed to locate the lines of the spectrum. The three MSB's are converted into eight voltage levels by the two operational amplifier circuits. These levels represent the eight major ranges of amu's. Thus, a zero level indicates that the mass spectrometer operates in the 0 to 31 amu range, while level seven signifies 224 to 255 range. The next five bits are converted into a 32 level signal, where each level represents one amu within the major range.

B. DATA CONVERSION AND MONITOR CIRCUITS

This group of circuits encompass a number of digital as well as linear devices. The three functional subgroups which are rather loosely related are shown in Figure 3. The two major subgroups are the data conversion and the PCM circuits respectively. The monitor circuits, with the exception of the D/A converters described in the previous sections of this report, are incidental to the control unit and serve mostly as buffers to isolate their signal sources from noisy umbilical lines during pre-launch operation.

The data conversion circuits convert the incoming pulse train of spectral information into an analog signal which in turn is converted into a digital form. The incoming signal has an amplitude of 15 volts and varies between 20 and 70 kpps. A voltage divider and an inverter are used to reshape and to reduce the signal to the 5 volt level. A voltage-to-frequency converter (VFC-32-SM)

is connected to perform frequency-to-voltage conversion. The output of the converter produces a signal between the limits of two and seven volts corresponding to the two extreme frequencies of the input. To remove the conversion ripple, a fourth order Butterworth filter (U4) with a cut-off frequency of nearly 1 kHz is employed. The input stage shifts and attenuates the signal such that the output of the filter (7 of U4) varies between 0 and -10 volts. This analog representation of the spectrum is inverted and reduced to the five volt level required for transmission through the telemetry.

Once every millisecond, the zero to -10 volt signal is converted into a 10-bit digital number. The conversion commands (STRT) originate in the sequencer and are synchronized with the PCM. The digital signal in a serial form (SRO) is shifted by the synchronization pulses (SYNC) into a shift register (U30, U31) for a temporary storage. Two hundred microseconds after the conversion has been initiated, the digital word is transferred in parallel into another shift register (U32, U33). The serial output (DATA), MSB first, is transmitted at the rate of the PCM clock to a gate in the sequencer section. Coinciding with the end of the LSB a new data word is once again loaded into the shift register by the P/S-2 pulse.

The rest of the PCM signal is generated by the third shift register (U35 - U38). Upon a command from the sequencer (P/S-1) the data present on the parallel input lines is loaded into the

circuit. The MSB of the 16-bit synchronization pattern 111010 1110010000 appears at the output (ID) of this circuit signalling the start of a new PCM frame. The bias, mode and the nine MSB's of the up-counter, all originating in the control section, are loaded into the last two registers. The PCM clock converts the stored data into the serial format of the PCM. This process is repeated once every 12 milliseconds. The output signal also goes to a gate in the sequencer section where it is combined with the DATA sequence to form one complete frame of the PCM.

C. THE SEQUENCER

Clock and synchronization pulses to coordinate the various functions of the control unit originate in the group of circuits shown in Figure 4. Mostly counters, flip flops and a few gates are used to generate and space the pulses. The timing diagrams of the more significant waveforms are presented in Figure 5.

The waveforms are derived from a C-MOS crystal controlled oscillator (U1) operating at 80 kHz. An external clock of a different frequency may be substituted through U2 for debugging, testing, or some other purposes during the adjustment and the calibration process of the mass spectrometer. Counters U3, U4, and U5 scale down the master clock frequency. The inverted 10 kHz PCM clock originates at pin 13 of U3 (13U3). A stream of 200 μs pulses with a period of one millisecond are generated at 6U4. The period of the AMU clock at the output of the divide by six counter (12U5) is 750 μs. This is the signal which clocks

the up-counter in the control section. The AMU CLK waveform is once more divided by 16 (6U3). The resulting waveform is used to trigger the counter U6. Since the transitions of the described waveforms coincide with the negative-going edge of the master clock signal, the U6 unit is again reset 6 μs later by the high level of the master clock. This process repeats itself every 12 ms. During that time, the up-counter advances by 16 counts. Thus the pulse at 3U6 marks the beginning of every new sweep through one amu range by the mass filter. This marker pulse is also used to reset the frequency dividers. Therefore, a complete synchronization and timing of all waveform transitions are maintained.

When a ONE is present on the SWP line, the request for digital control signal updating originates at the comparator circuits in the control section. Transition from ZERO to ONE on COMP line triggers 13U9 into a ONE state. The next amu marker pulse is allowed to pass through the AND gate (N1) and clocks 2U9 to ZERO.

Normally the two pulses, the amu marker and the comparator output, coincide. In an event that the comparator were to produce an early indication that an assigned sweep has been completed, the circuit will not respond until the next marker signal. Therefore, the updating process will always take place only after a sweep through the whole region assigned to one amu has been completed. This minimizes the possibility of confusion in the interpretation of the PCM data where under premature updating the amu identification word may not represent the data in that frame.

Once a ZERO appears at 9N3, the master clock signal passes through that gate and appears inverted at 12U13 as the A CLK which advances the address counter. The counter is advanced at the negative going edge of a clock pulse. Since the described events take place when the master clock signal is low, the address counter first sees a high level at its clock input and remains in its original state. Also, since at that time, A_1 and A_0 are both low, a ONE is present on line S_1. This is the strobe pulse which stores the contents of the memory appearing on the output bus into the first latch. As long as the gate 10N3 passes the master clock, the address counter advances while the strobe pulses are sequentially generated on the appropriate lines whenever the master clock signal is low.

At the start of the updating process when 2U9 becomes ZERO, its complement at 1U9 clocks 1U8 into ONE state, and thus, the signal PE to preset the up-counter is generated. It remains present until S_4 resets the flip flop. Meanwhile, the output 12U8 which was reset to ONE by the first strobe pulse (S_1) is again set to ZERO by the third strobe pulse of the sequence (S_3) thereby blocking S_4 from the reset inputs of U9. The 10N3 gate remains open and once again S_1 resets 12U8. During this second sequence of the updating process, PE is absent. Therefore, S_4 is able to terminate the process by resetting U9.

When the SWP line is low, the updating process may be initiated without the benefit of the comparator by the amu marker pulse origin-

ating at 2N1. This time the gate 4N2 is blocked to the S_3 pulse. Therefore, the process terminates shortly after the fourth strobe pulse (S_4) appears on the line.

To initiate the analog-to-digital conversion and to control the transfer of the digital data from the temporary storage register into the output register, two signals, START and P/S-2 are generated by U7. The positive and the negative going edges of the one kHz 200 μs pulse train continuously clock the outputs 3 and 11 respectively of that dual counter into the high state. The master clock continuously resets them 6 μs later. Therefore, two pulse trains displaced by 200 μs from each other are available to control at a 1 kHz rate the sampling and the transfer of data.

The P/S-1 pulse marks the beginning of the PCM synchronization pattern. It originates at 1U11. The P/S-2 pulse triggers 13U11 into the ONE state which in turn clocks 1U11 high. Once again, the master clock pulse resets 1U11 6 μs later. This process occurs once every 12 ms and coincides with the first P/S-2 pulse appearing one millisecond after the amu marker pulse which resets the 13U11 into the ZERO state.

To combine the ID and the DATA portions of the PCM signal, yet another counter U10 is utilized. P/S-2 signal pulses the counter while P/S-1 resets it. When in reset state, 7U10 is low. Therefore, the ID signal is passed through the analog gate 2U12 to the output. Three P/S-2 pulses (3 ms) later 7U10 goes high, closes the ID gate and opens the DATA gate. The U10 counter

disables its clock input and once again awaits the reset signal. During the three milliseconds that the ID gate remains open, 30 PCM pulses which include synchronization pattern, status and amu identification bits pass to the output. During the remaining 9 ms the 90 spectrum data bits are transmitted.

The same analog gate unit also controls the frequency of the AMU CLK. During the total ions mode, the dc component of the quadrupole excitation signal is reduced to ZERO while the RF component is held at a constant level. When this mode of operation is necessary, the TOT ION line is set to ZERO. Gate 4 of U12 connects the waveform which generates the amu marker to the up-counter. Since this square wave has a period of 12 ms, the up-counter remains in its present state for that duration. Therefore, a constant RF level is generated during that time. At the end of this period, the amu marker pulse or the comparator pulse initiate another updating process.

When a need arises to change the quadrupole control program during a flight, a ZERO is stored in the memory to appear on the PM line during each cycle of the program which is to be replaced after a predetermined number of cycles. The negative transitions advance the counter U41. The four LSB's select one channel of the 16 channel multiplexer/demultiplexer U42. ONE appears in the selected line P_0 through P_{15} once every 16 PM pulses. The next four bits control another multiplexer U44. Lines P_{16} through P_{31} are sequentially connected to the output (1U44). A new line is selected every 16 PM pulses. Therefore, when appropriate P_0 through P_{15} lines are

connected to the P_{16} through P_{31} lines, a ONE is generated at 1U44 after the required number of PM pulses. These pulses trigger the program counter 9U6. The outputs of this counter generate the three MSB's of the memory address. In this manner, the eight different programs stored in the EPROM may be sequentially selected. The total number of PM pulses is restricted to less than 255 before the counter U41 recycles. There may be instances when a recycling operation is desirable.

The control unit is reset at power turn on. Another reset occurs when the RF and the HV power is turned on. This marks the start of the data collection period. These reset pulses are generated by the circuit designated as PWR RST and RF RST respectively. There is a programmed reset (PR) capability. Whenever this line makes a transition from ZERO to ONE, the unit is resynchronized and the address counter is reset to the 0000000 address of the program in which it was operating. The program counter can be reset only by the power turn on pulses. This programmed reset may be utilized as a simple instruction to start a program cycle from the beginning. Also, if by chance the address counter were to enter an unprogrammed portion of the memory, it would generate a reset and it would return to the beginning of the program.

IV. CONCLUSION

A system has been developed to control digitally the functions of a quadrupole mass spectrometer. Included are the provisions to transmit the data obtained from the mass filter in an analog as well as in a digital form.

The design of the system provides for a complete synchronization between the PCM and the control functions of the mass filter. Thus, a well defined time relationship between the generation, sampling and transmission of the data are maintained at all times. To suit the requirements of the rapidly changing environment during a rocket flight, a limited number of prearranged control programs may be selected. Only seven jumper wires between the pins of a connector are required to accomplish that task. Therefore, the connector may be wired and installed just before the final elevation of the vehicle, when the expected changes in the flight trajectory due to atmospheric conditions have been determined.

The design is based on a single eight kilobit EPROM. This provides for eight different control programs of 16 breakpoints each. To extend that capability to 32 breakpoints per program or to 16 programs of 16 breakpoints, the present EPROM may be replaced by one with 16k bit capacity. Only a minor wiring change is required.

In the event that the sequential control program selection becomes unacceptable, the single plug control may be replaced by an EPROM circuit. In that case, the outputs of the EPROM would

bypass the program counter and would directly control the most significant address bits of the EPROM containing the programs. Another step could be taken and a provision could be included to program the newly introduced EPROM over the umbilical cable. This, of course, would require more elaborate circuit arrangements, expecially if serial address and data transmission were contemplated to minimize the number of umbilical lines.

Although this control unit has been designed specifically for the control of a mass spectrometer, it may be adapted with or without modifications for other applications. It may be used to control other instruments and to convert their data into a PCM format, or in simplified form, it could be employed as a sequencer-timer to provide timing functions for an entire rocket payload.

PERSONNEL

A list of the engineers and technicians who contributed to the work reported:

J. Spencer Rochefort, Professor of Electrical Engineering, Principal Investigator.

Raimundas Sukys, Senior Research Associate, Engineer.

Thomas Palasek, Research Assistant, Engineer.

Richard H. Marks, Technician, Electrical Engineering.

RELATED CONTRACTS AND PUBLICATIONS

F19628-74-C-0042	1 September 1973 through 31 August 1976.
F19628-76-C-0256	1 September 1976 through present.

Sukys, R. and Goldberg, S. (1974), "Control Circuits for a Rocket Payload Neutralization and Other Topics", AFCRL-TR-74-0580.

Sukys, R., Rochefort, J. S. and Goldberg, S. (1975), "Bias and Signal Processing Circuits for a Mass Spectrometer in the Project EXCEDE: SWIR Experiment", AFGL-TR-76-0060.

Rochefort, J. S. and Sukys, R. (1976), "Instrumentation Systems for Mass Spectrometers", AFGL-TR-76-200.

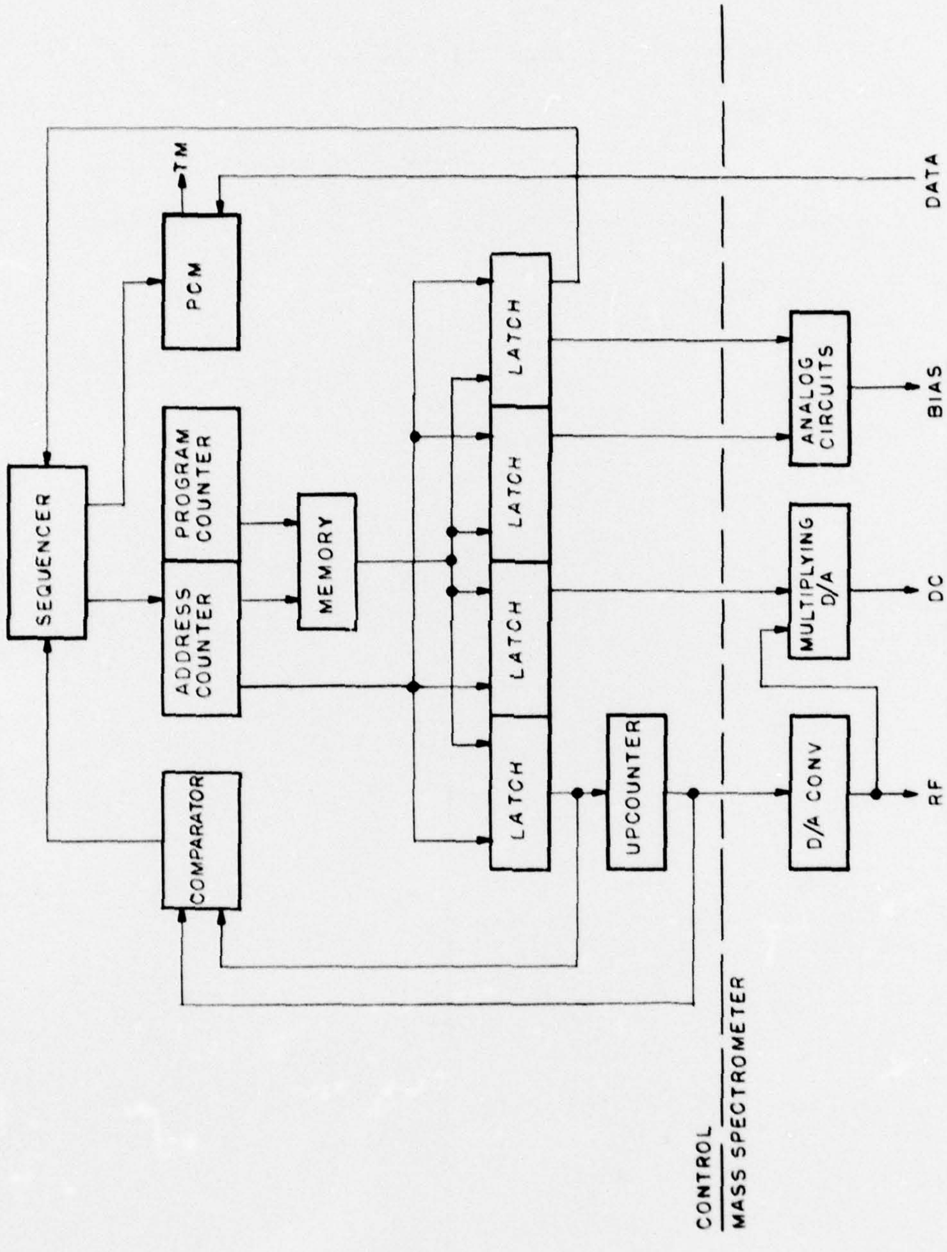
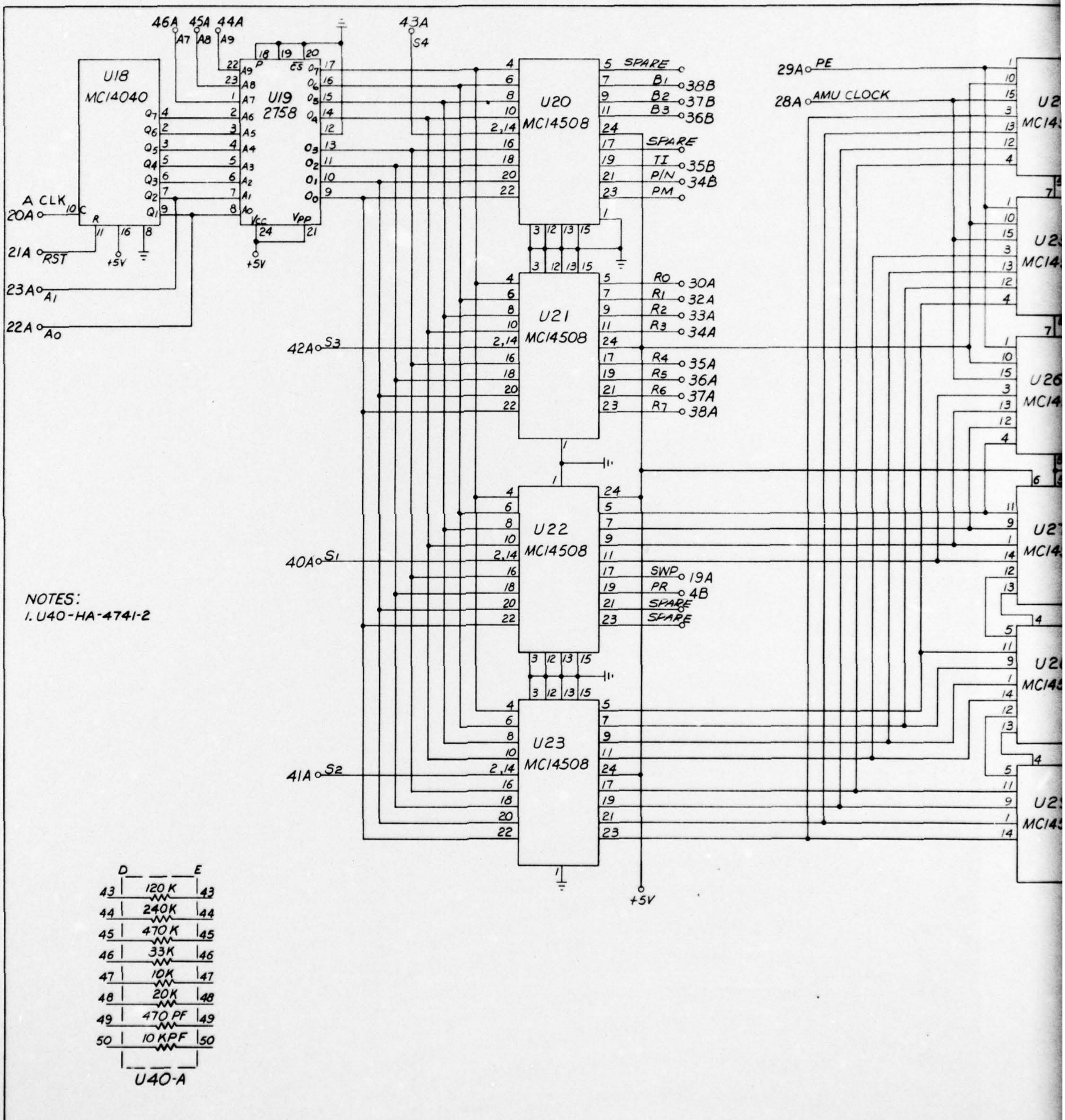


FIGURE 1. GENERAL BLOCK DIAGRAM OF CONTROL UNIT


U18
MC14040
U19
2758
U20
MC14508
U21
MC14508
U22
MC14508
U23
MC14508
A CLK
20A
21A RST
23A A1
22A A0
46A 45A 44A
43A S4
42A S3
40A S1
41A S2
29A PE
28A AMU CLOCK
SPARE
B1 38B
B2 37B
B3 36B
TI 35B
P/N 34B
PM
R0 30A
R1 32A
R2 33A
R3 34A
R4 35A
R5 36A
R6 37A
R7 38A
SWP 19A
PR 4B
+5V
NOTES:
1. U40-HA-4741-2
120 K
240K
470 K
33K
10K
20K
470 PF
10 KPF
U40-A

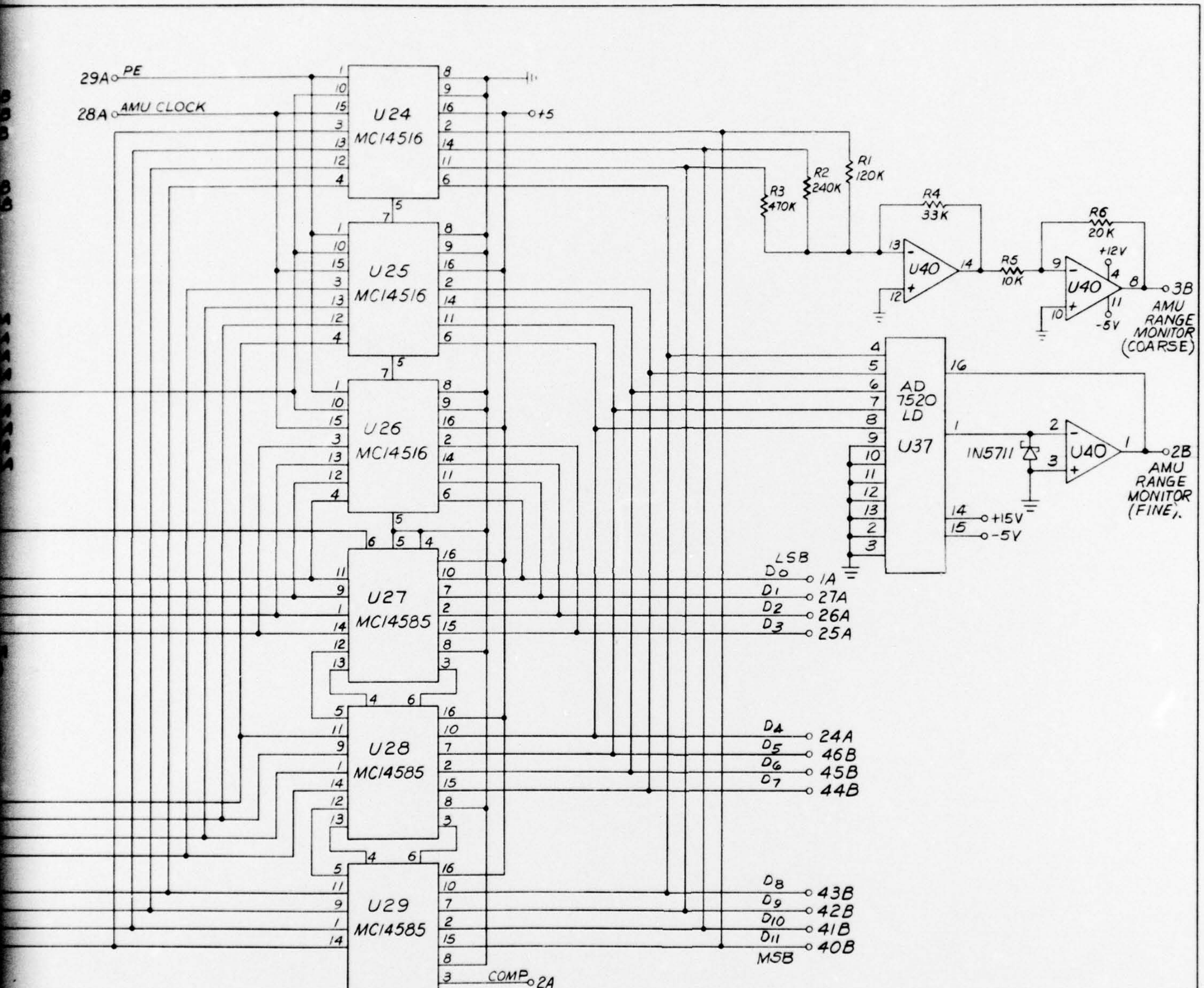


FIGURE 2

TOLERANCE UNLESS OTHERWISE NOTED

DECIMAL: ± .01 ± .005

FRACTIONAL: ± 1/64

ANGULAR: ± 0° 30'

SURFACE FINISH: 125 √

BREAK ALL SHARP EDGES AND DEBURR

FINISH

APPLICATION

DRAWN R.S. EVELAN

DATE 4-17-78

SCALE

MATERIAL

CONTROL CIRCUITS

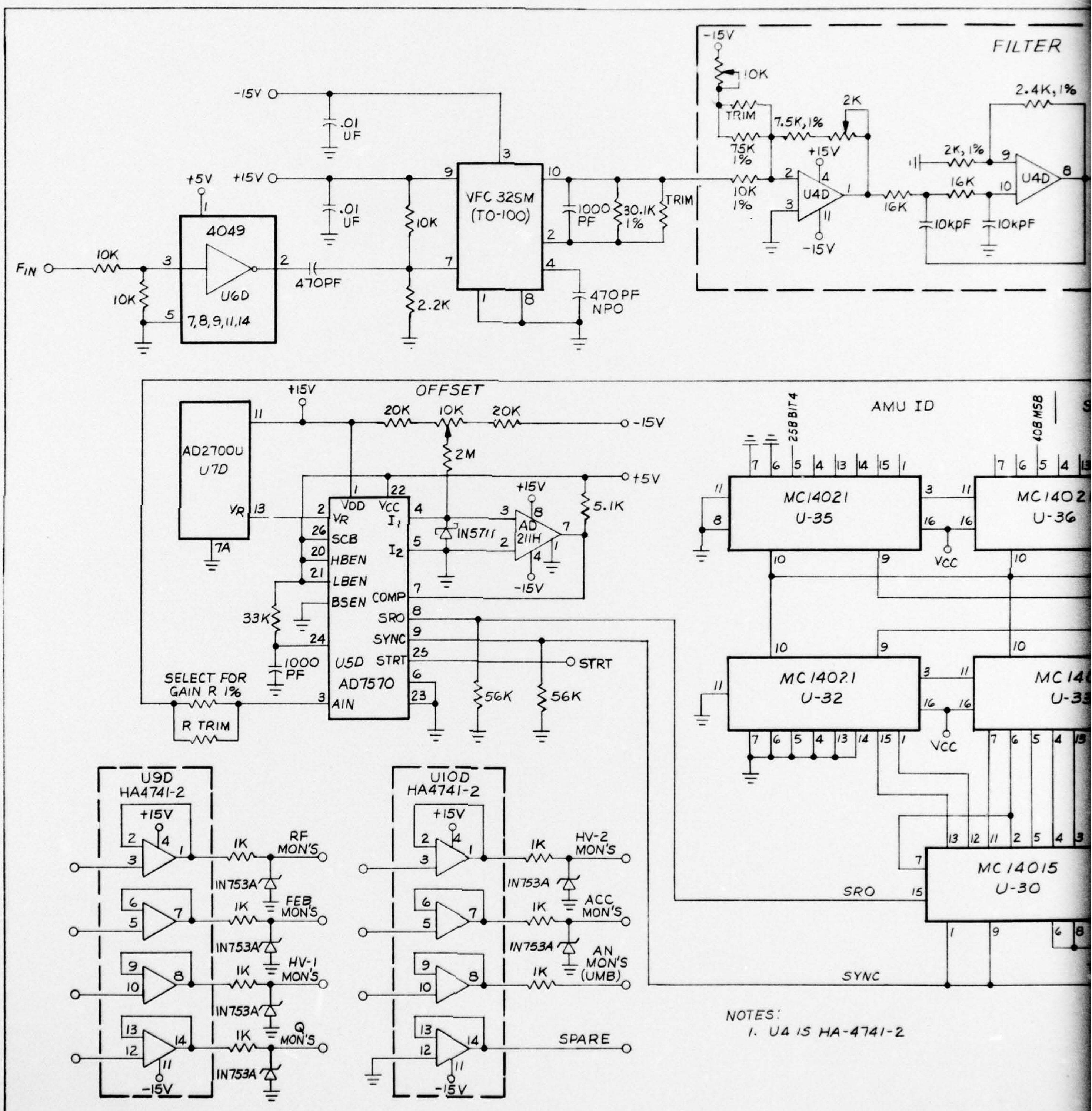
CONTRACT NUMBER

NORTHEASTERN UNIVERSITY

ELECTRONICS RESEARCH LAB

COLLEGE OF ENGINEERING

BOSTON, MASS. 02115


FILTER
-15V
10K
TRIM
7.5K, 1%
2K
75K 1%
10K 1%
+15V
U4D
2K, 1%
16K
2.4K, 1%
10kpF
-15V
+5V
+15V
.01 UF
4049
U6D
7,8,9,11,14
FIN
10K
470PF
2.2K
VFC 32SM (TO-100)
1000 PF
30.1K 1%
TRIM
470PF NPO
OFFSET
20K
10K
20K
2M
5.1K
AD2700U U7D
VR
7A
VDD
VCC
VR
SCB
HBEN
LBEN
BSEN
COMP
SRO
SYNC
STRT
AIN
U5D AD7570
IN5711
AD 211H
33K
1000 PF
SELECT FOR GAIN R 1%
R TRIM
56K
STRT
AMU ID
25B BIT 4
40B MSB
MC14021 U-35
MC14021 U-36
MC14021 U-32
VCC
MC14015 U-30
SRO
SYNC
U9D HA4741-2
U10D HA4741-2
1K
RF MON'S
FEB MON'S
HV-1 MON'S
Q MON'S
HV-2 MON'S
ACC MON'S
AN MON'S (UMB)
SPARE
IN753A
NOTES:
1. U4 IS HA-4741-2

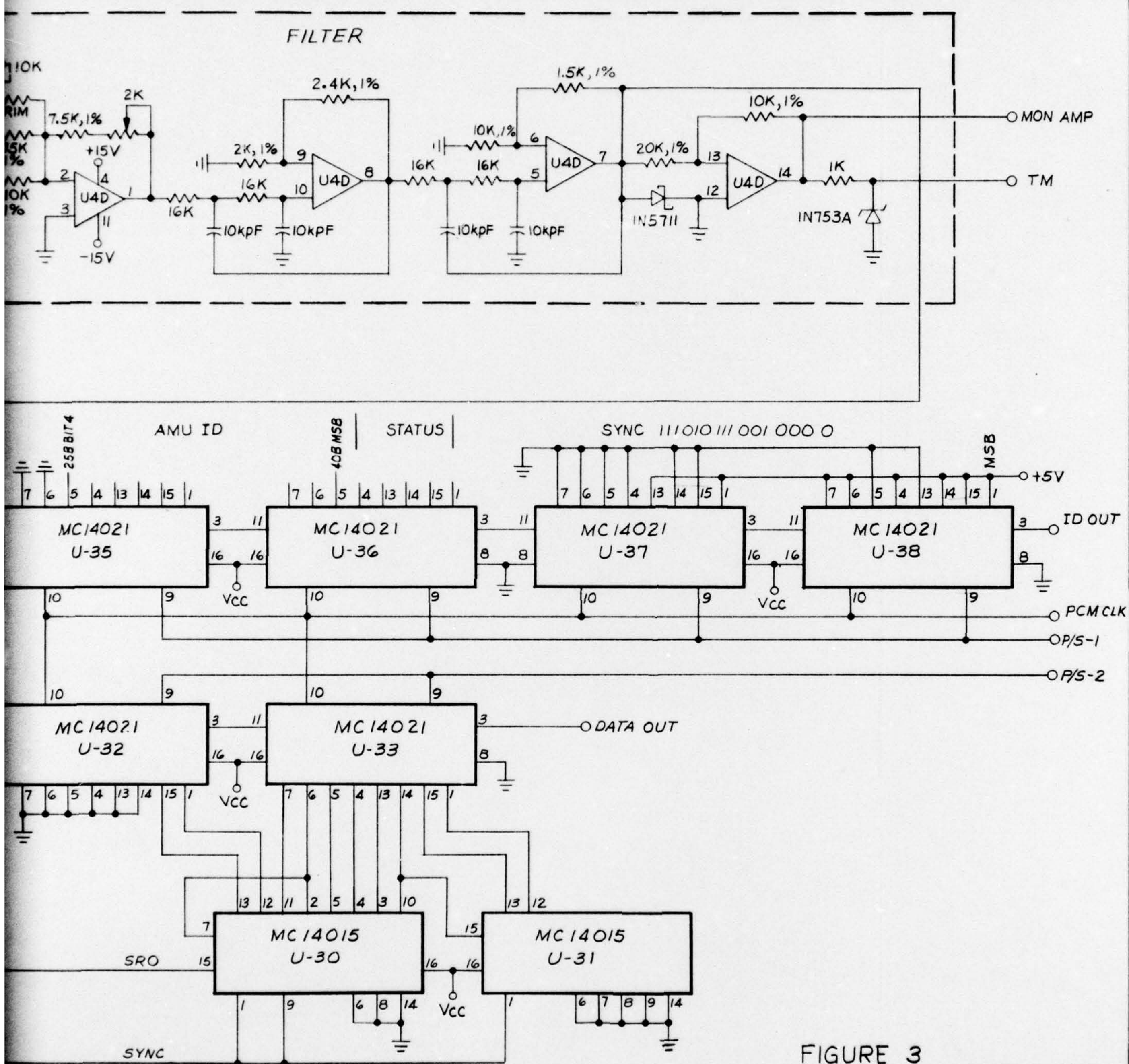
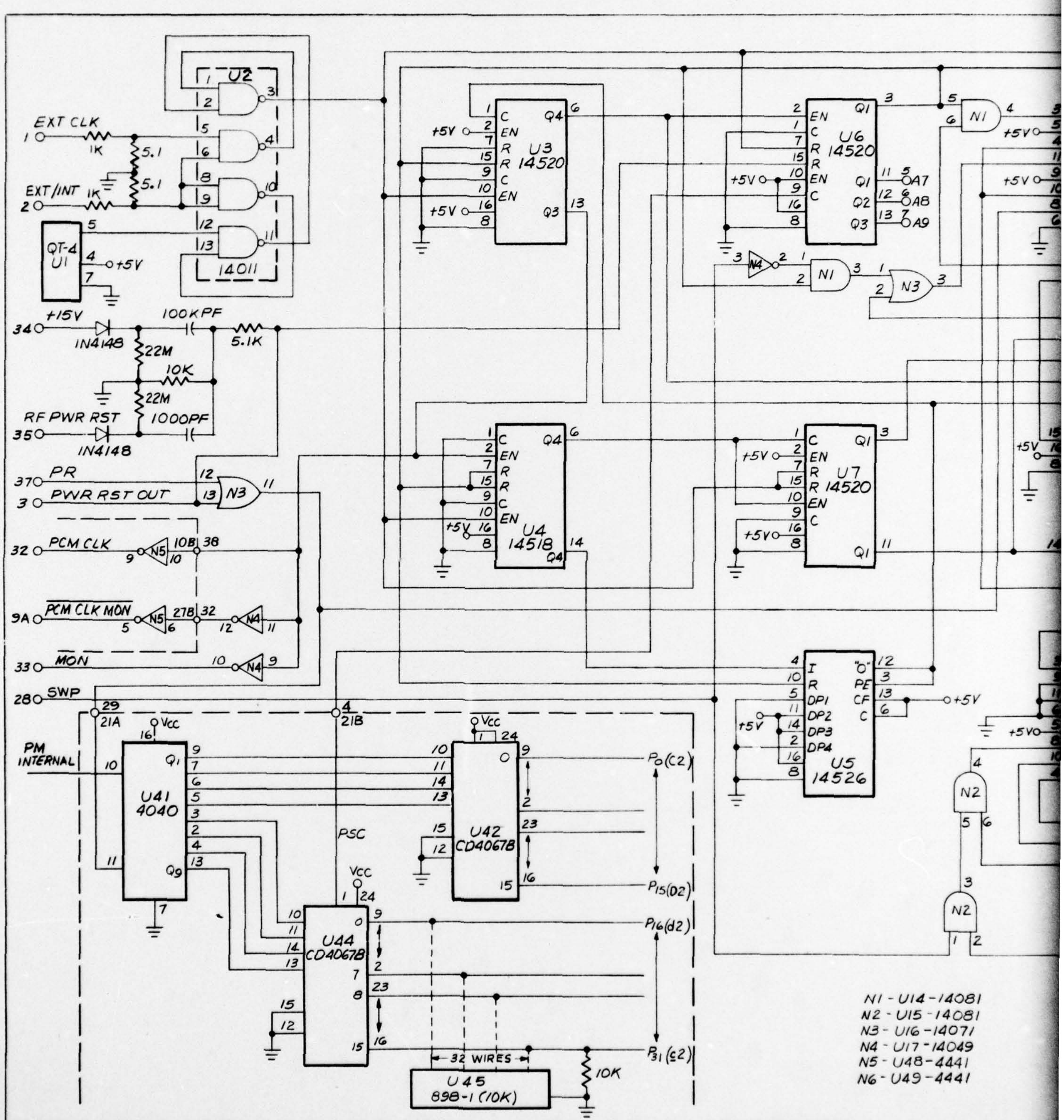


FIGURE 3

NOTES:
1. U4 IS HA-4741-2

TOLERANCE UNLESS OTHERWISE NOTED: DECIMAL: ± .01, ± .005; FRACTIONAL: ± 1/64; ANGULAR: ± 0° 30'; SURFACE FINISH: 125√; BREAK ALL SHARP EDGES AND BURRS	DRAWN: R.S. EVELYN	DATE: 3-28-78	NORTHEASTERN UNIVERSITY ELECTRONICS RESEARCH LAB COLLEGE OF ENGINEERING BOSTON, MASS. 02115
APPLICATION: NEXT ASSY / PROJECT	CHECKED / SCALE / MATERIAL	DATA CONVERSION CIRCUITS	CONTRACT NUMBER



EXT CLK
EXT/INT
1K
5.1
U2
14011
QT-4
U1
+5V
+15V
1N4148
100KPF
5.1K
22M
10K
1000PF
RF PWR RST
PR
PWR RST OUT
N3
PCM CLK
N5
PCM CLK MON
N4
MON
SWP
PM INTERNAL
U41
4040
U42
CD4067B
U44
CD4067B
PSC
VCC
32 WIRES
U45
898-1 (10K)
P0(C2)
P15(D2)
P16(d2)
P31(c2)
U3
14520
U4
14518
U6
14520
U7
14520
U5
14526
N1
N2
A7
A8
A9
N1 - U14 - 14081
N2 - U15 - 14081
N3 - U16 - 14071
N4 - U17 - 14049
N5 - U48 - 4441
N6 - U49 - 4441

1

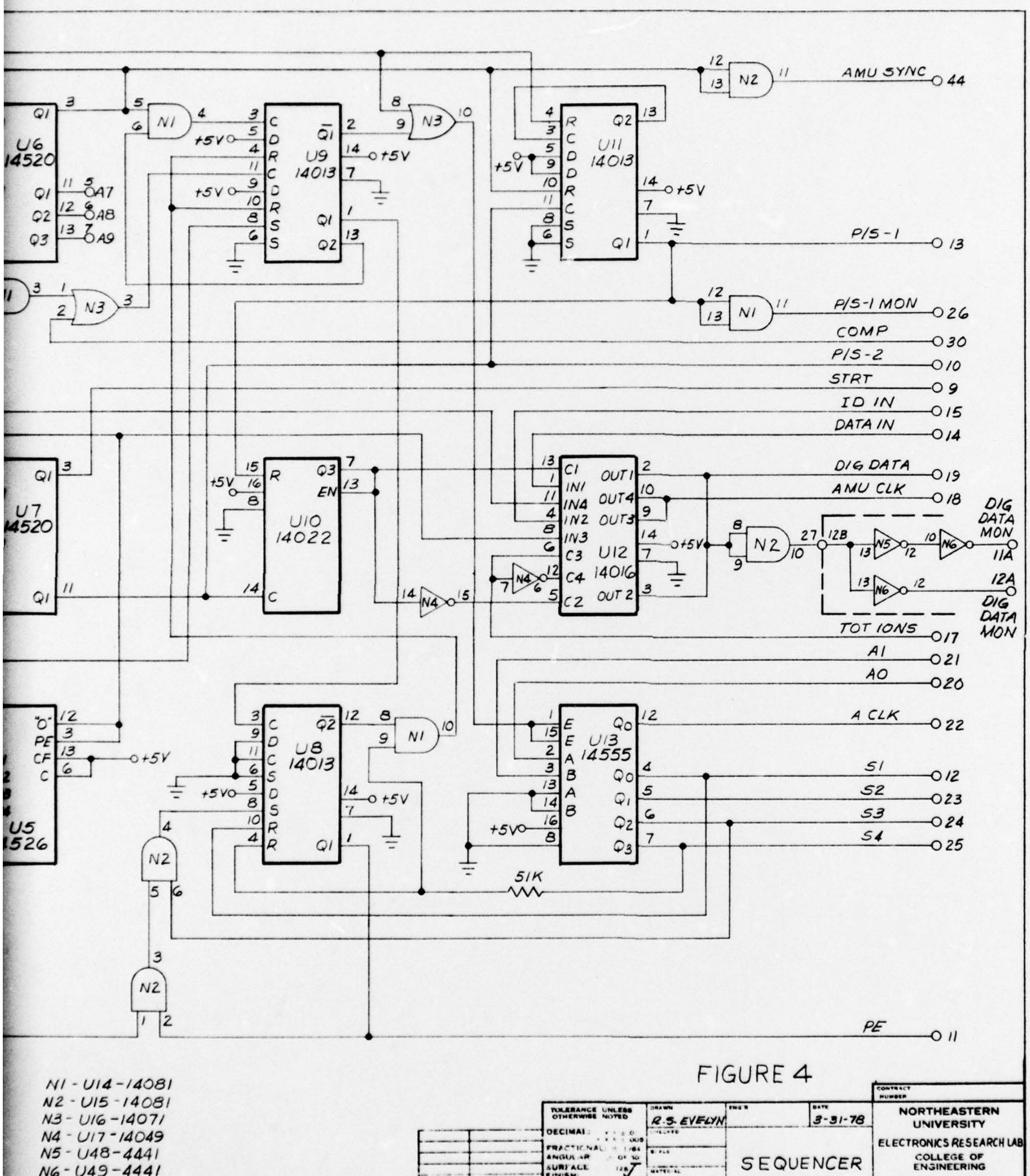


FIGURE 4

TOLERANCE UNLESS OTHERWISE NOTED	DRAWN R.S. EVELYN	DATE 3-31-78	NORTHEASTERN UNIVERSITY ELECTRONICS RESEARCH LAB COLLEGE OF ENGINEERING BOSTON, MASS. 02115
APPLICATION	SEQUENCER CIRCUITS		

2

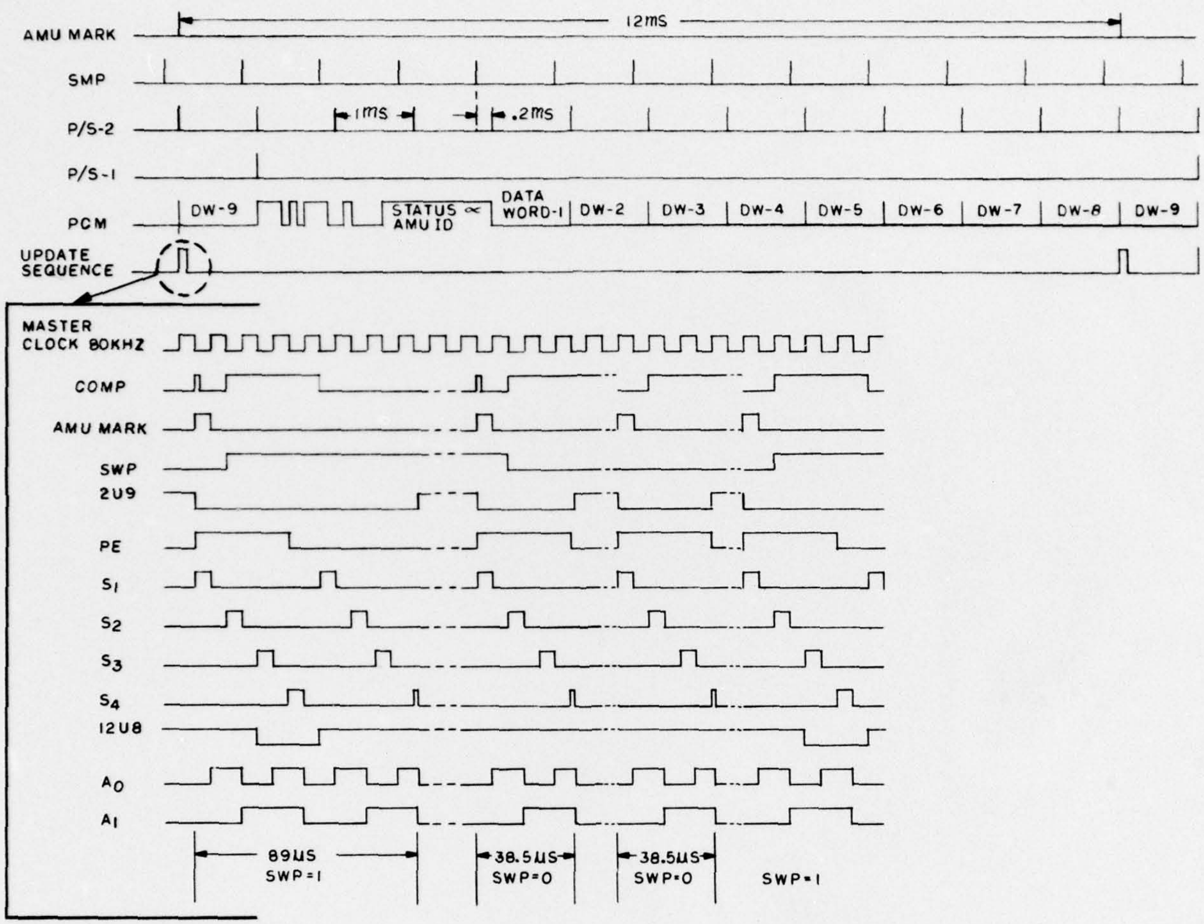


FIGURE 5. SEQUENCER AND PCM WAVEFORMS